Application Note	AN-MEGA-0011-v101EN

Brake control signal for closed loop applications using Customizable Logic

Inverter type	FRENIC MEGA
Software version	1000, 2000 and 2100 ONLY
Required options	-
Related documentation	MEGA_IM_AE_1335a-E
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Use	Public, Web
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Version	1.0.1
Languages	English

1. Introduction.

This document describes how a new variant of brake control signal for closed loop applications is programmed using Customizable Logic of FRENIC MEGA. The main difference (advantage) of this signal is that is not turned OFF (brake applied) every time the motor reaches zero speed if the RUN command is kept ON. This behaviour has been already implemented in the fourth software and later versions of MEGA. Therefore it is only required to make the solution described in this document when using FRENIC MEGA inverters with third software version (ROM 1000, 2000 and 2100).

2. Implementation Idea.

The main ideas of this implementation are:

- The brake signal takes into account the RUN command, the RUN status and the output frequency:
  - If the RUN command is given to the inverter the brake signal will be open after RUN status confirmation by the inverter. The brake will not be opened if there is no RUN status confirmation (for example inverter is not enabled).
  - If the RUN command (FWD or REV) and the RUN status are kept ON the brake signal is not turned OFF (even at zero speed/frequency).
  - If the RUN command is turned OFF the brake signal is turned OFF after going under the frequency level configured (using FDT signal).
- If the inverter is NOT READY (for example inverter failure) the brake signal is turned OFF immediately.

Figure 1 shows the logic diagram of the brake control signal implementation.

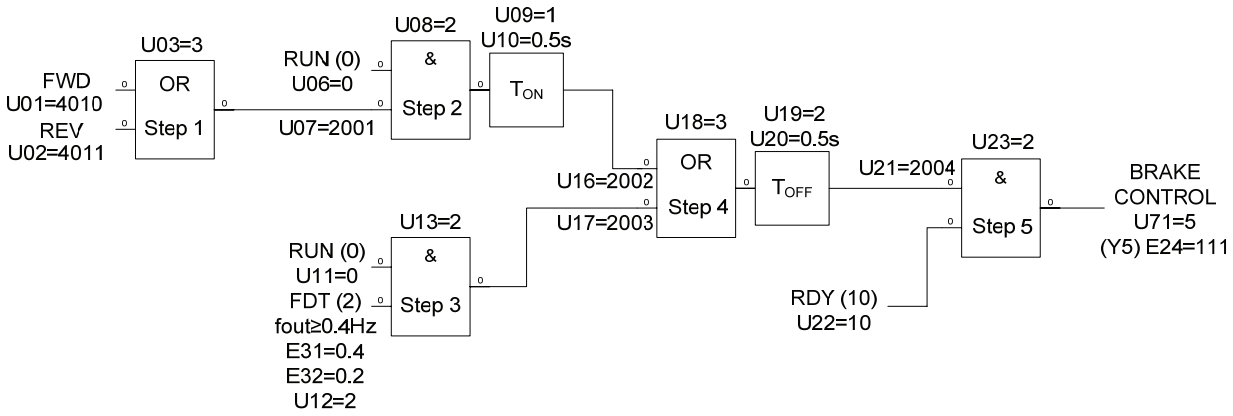

Figure 1. Logic diagram of the brake control signal implementation.

Table 1 shows the function codes different from default settings.

Table 1. Function codes different from default settings.

Function	Value	Description
U00	1	Enable Customizable Logic
U01	4010	Terminal [FWD] as input signal of step 1
U02	4011	Terminal [REV] as input signal of step 1
U03	3	OR + General-purpose timer for step 1
U06	0	RUN signal as input signal of step 2
U07	2001	Output of step 1 as input signal of step 2
U08	2	AND + General-purpose timer for step 2
U09	1	ON-delay timer for step 2
U10	0.5 s	Time for the ON-delay timer of step 2.
U11	0	RUN signal as input signal of step 3
U12	2	FDT signal (configured by E31 and E32) as input signal of step 3
U13	2	AND + General-purpose timer for step 3
U16	2002	Output of step 2 as input signal of step 4
U17	2003	Output of step 3 as input signal of step 4
U18	3	OR + General-purpose timer for step 4
U19	2	OFF-delay timer for step 4
U20	0.5 s	Time for the OFF-delay timer of step 4
U21	2004	Output of step 4 as input signal of step 5
U22	10	RDY signal as input signal of step 5
U23	2	AND + General-purpose timer for step 5
U71	5	Customizable logic output signal 1 is out of step 5
E24	111	Y5A/C relay output is controlled by customizable logic output signal 1
E31	0.4	FDT signal level
E32	0.2	FDT signal hysteresis
d24	1	Zero speed control enabled at start up
F38	1	Stop frequency detection by commanded speed

This solution can only be used in closed loop applications (F42=6, PG vector control) because in this control mode the inverter is able to keep full torque at zero speed (the motor can hold the load at standstill and therefore is not required to apply the brake when the inverter is in RUN state).

3. Conclusion.

Using Customizable Logic of FRENIC MEGA we can create a special brake control signal required for some applications in closed loop (crane hoists, robots,…). This special control signal has been already included in later software versions of FRENIC MEGA.

4. Document history.

Version	Changes applied	Date	Written	Checked	Approved
1.0.0	First version	27/08/2010	D. Bedford		
1.0.1	F38 has been added	29/09/2010	D. Bedford	JM. Ibáñez	D.Bedford