Application Note	AN-MEGA-0014-v103EN

Solar Pump with Dry Well detection using Customizable Logic of FRENIC MEGA

Inverter type	FRENIC MEGA
Software version	3700 or later
Required options	-
Related documentation	MEGA_IM_AE_1335a-E
Author	Joan Manel Ibañez
Use	Public, Web
Date	29/08/2011
Version	1.0.3
Languages	English

1. Introduction.

This document describes the implementation of a function using Customizable Logic of FRENIC MEGA to detect that the Well is Dry, to be used in Solar Pumping Application.

FRENIC MEGA can be supplied by a Solar Cell in order to control an induction motor that moves a pump to extract water from a well. The rotating speed (frequency) of the pump will depend on the available power, by using a PID control loop that monitors the voltage of the inverter DC bus (as shown in figure 1). On the other hand, it is important to prevent that the pump rotates when the well is dry, otherwise the pump will be damaged (overheated due to the friction).

2. Implementation Idea.

The main ideas of this implementation are:

- The output frequency (rotation speed of the pump) depends on the available power. This is implemented by using a PID controller that compares the inverter DC link voltage with a fixed set-point (as shown in figure 1).
- If the output frequency stays continuously at a certain frequency (configurable) **f1** during a time (configurable) **T1**, the pump must stop because it means that it is NOT pumping water (in other words, the well is dry).
- The inverter keeps in stop mode for a time (configurable) **T2**.
- After time **T2** has elapsed, the pump starts again and checks again the first condition. The cycle runs continuously.
- If RUN command (digital input FWD) is switched OFF and switched ON again then time **T2** is reset and the inverter starts immediately.
- The pump will not start until the DC link voltage is higher than a certain value **V1**, configurable by function J12 (in this example the percentage, 50 % is equivalent to 500 VDC).

NOTE: If response of PID is not fast enough for avoiding Undervoltage level, it is recommended to wait 10 minutes after the DC link bus has been reestablished before restarting inverter operation. Otherwise, expected inverter lifetime could be reduced due to stress on the DC Bus charging circuit.

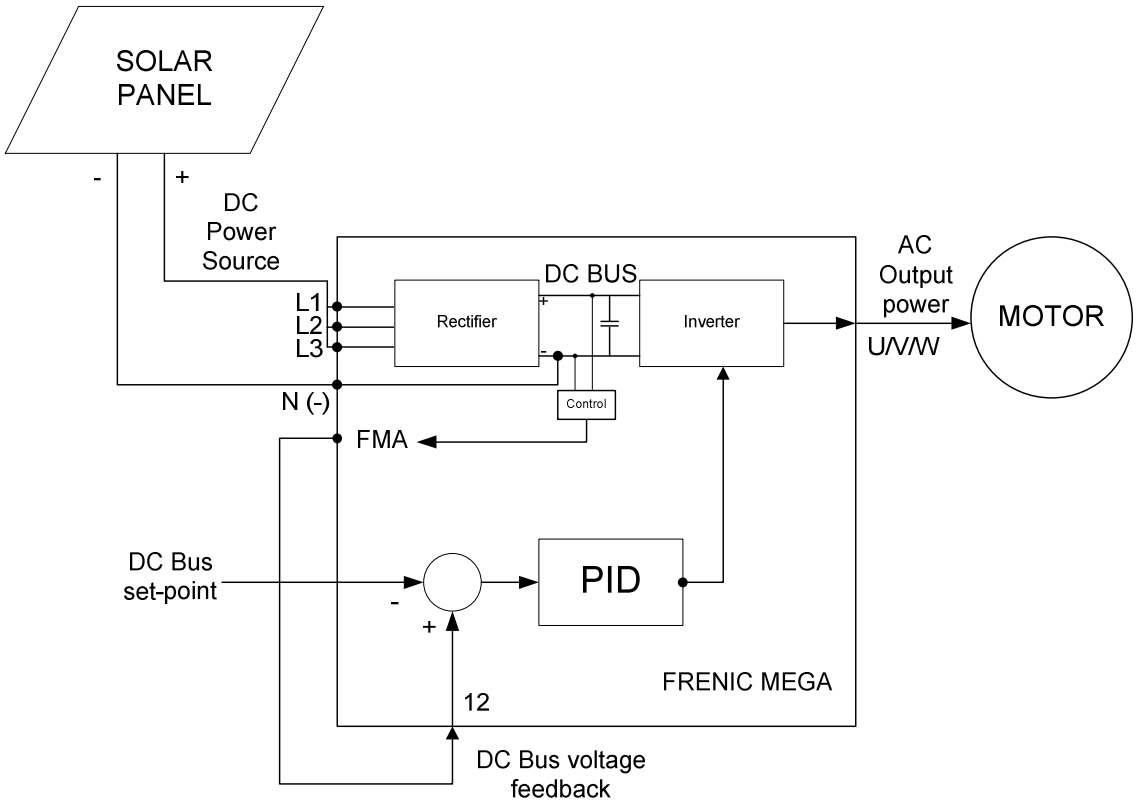
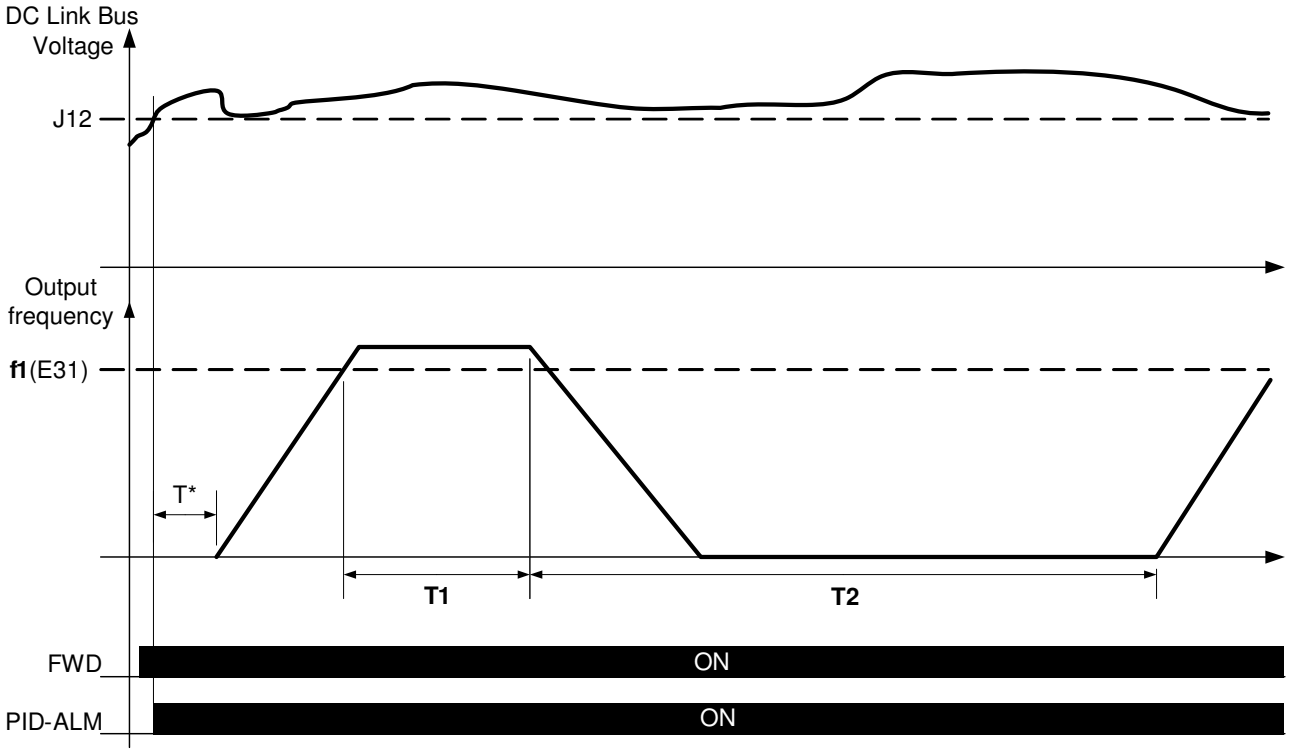
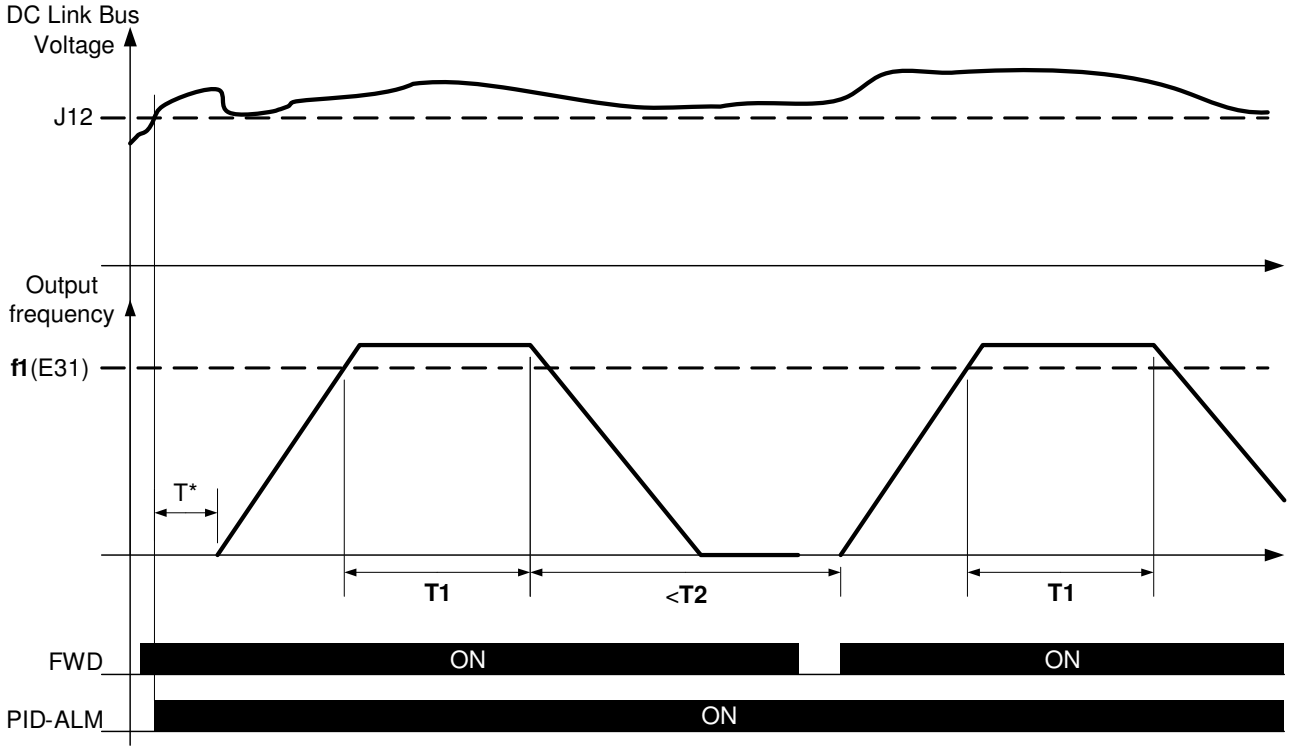


Figure 1. Frequency control depending on the available power



*Only if it's the first time since inverter power recovery or alarm

Figure 2. Dry well function sequence



*Only if it's the first time since inverter startup or alarm

Figure 3. Dry well function sequence. **T2** Timer Reset when FWD Terminal is removed

Figure 4 shows the logic diagram of the dry well detection function implemented.

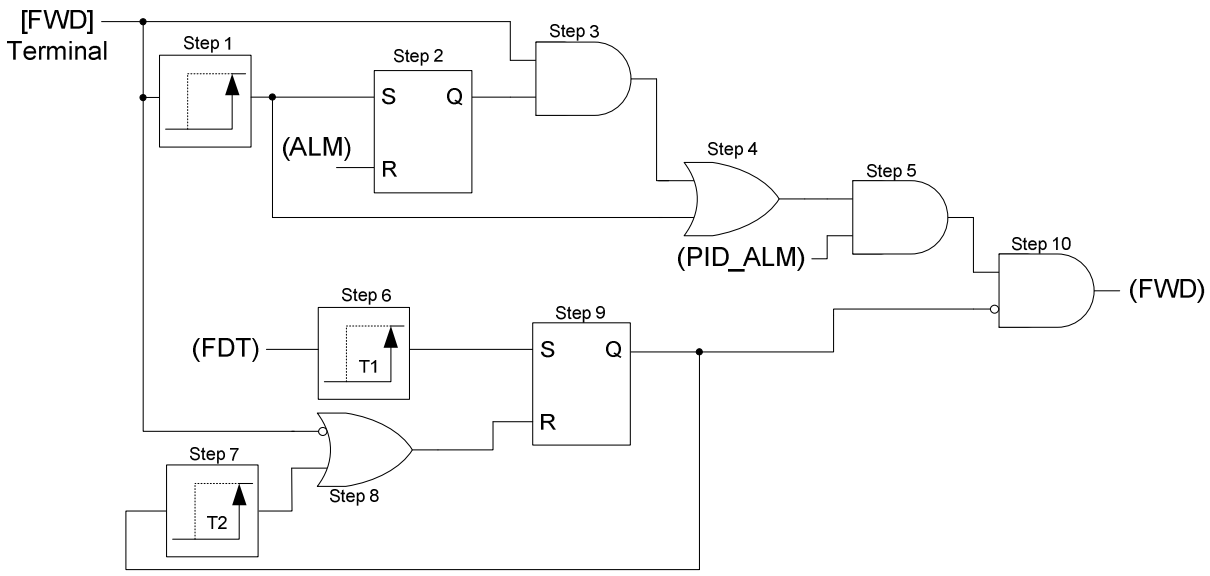


Figure 4. Logic diagram of the dry well detection function.

3. Connection diagram

Figure 5 shows the connection diagram.

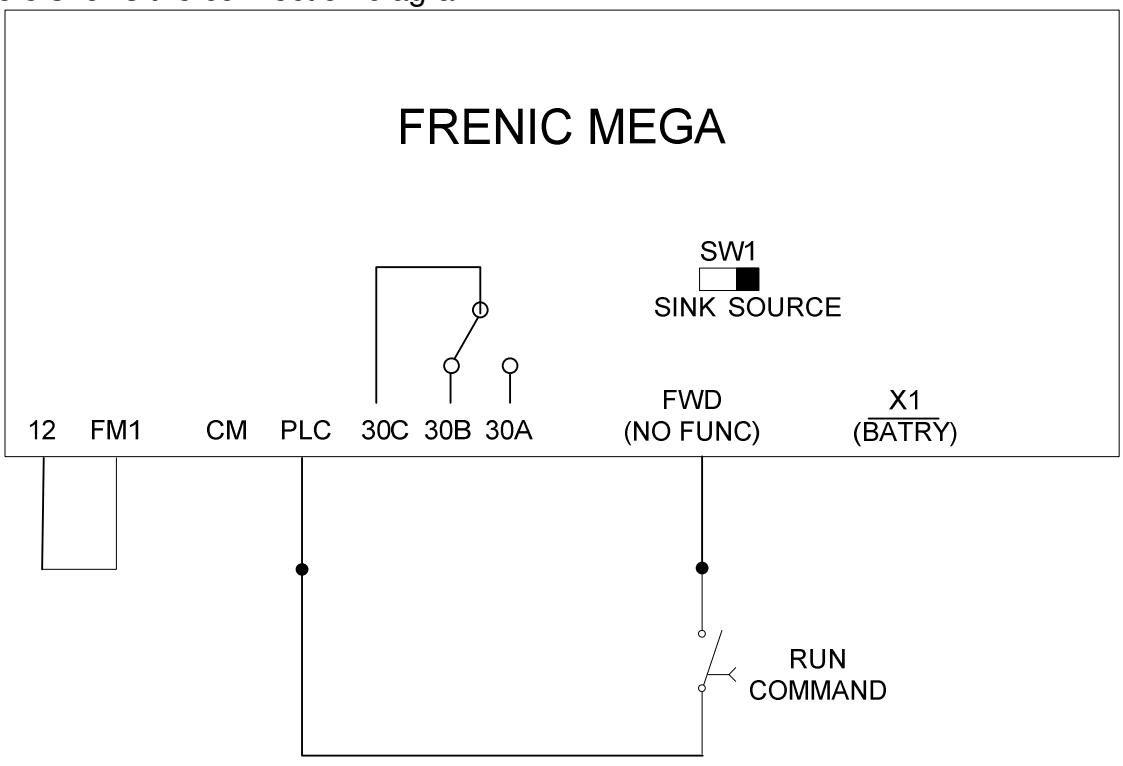


Figure 5. Connection Diagram

4. Parameter setting

The following tables show the function codes different from default settings.

Table 1. Function codes related to Dry Well detection function.

Function	Value	Description
U00	1	Enable Customizable Logic
U01	4010	Terminal [FWD] as input signal 1 of step 1
U03	1	Through output + General-purpose timer for step 1
U04	1	On-delay timer for step 1
U05	0.5 s	Time for the ON-delay timer of step 1
U06	2001	Output of step 1 as input signal 1 of step 2
U07	99	Any alarm as Input signal 2 of step 2
U08	5	Set priority flip-flop + General-purpose timer for step 2
U11	2002	Output of step 2 as input signal 1 of step 3
U12	4010	Terminal [FWD] as input signal 2 of step 3
U13	2	AND + General-purpose timer for step 3
U16	2001	Output of step 1 as input signal 1 of step 4
U17	2003	Output of step 3 as input signal 2 of step 4
U18	3	OR + General-purpose timer for step 4
U21	2004	Output of step 4 as input signal 1 of step 5
U22	42	PID alarm as input signal 2 of step 5
U23	2	AND + General-purpose timer for step 5
U26	2	FDT (configured with E31 and E32) as input signal 1 of step 6
U28	1	Through output + General-purpose timer for step 6
U29	1	On-delay timer for step 6
U30	15.00 s	Time for the ON-delay timer of step 6. Time **T1**
U31	2009	Output of step 9 as input signal 1 of step 7
U33	1	Through output + General-purpose timer for step 7
U34	1	On-delay timer for step 7
U35	30.00 s	Time for the ON-delay timer of step 7. Time **T2.**
U36	2007	Output of step 7 as input signal 1 of step 8
U37	5010	Terminal [FWD] inverted as input signal 2 of step 8
U38	3	OR + General-purpose timer for step 8
U41	2006	Output of step 6 as input signal 1 of step 9
U42	2008	Output of step 8 as input signal 2 of step 9
U43	5	Set priority flip-flop + General-purpose timer for step 9
U46	3009	Output of step 9 inverted as input signal 1 of step 10
U47	2005	Output of step 5 as input signal 2 of step 10
U48	2	AND + General-purpose timer for step 10
U71	10	Customizable logic output signal 1 is out of step 10
U81	98	Customizable logic output signal 1 function is FWD
E31	50.0 Hz	Frequency Detection 1 Level. Used as the frequency level **f1** to stop the pump. Can not be higher than functions F03 and F15. If needed to increase E31 beyond these functions then increase also F03 and F15.
E32	1.0 Hz	Frequency Detection 1 hysteresis width.

Table 2. Additional settings related to the frequency control.

Function	Value	Description
J01	2	PID control inverse operation
J03	1.0	PID controller proportional gain
J04	0.1	PID controller integral time
J12	50 %	Upper level PID alarm. DC link voltage level **V1** that allows to start the pump.
J57	57 %	PID control set point
F30	9	Output of FM1 is DC link voltage
E61	5	Terminal 12 used as PID feedback

Table 3. Additional settings related to the Low Voltage operation

Function	Value	Description
E01	1059	X1 configured as BATRY signal inverted to cancel Low voltage Alarm

5. Conclusion.

FRENIC MEGA can be applied to Solar Pump application successfully. Using Customizable Logic of FRENIC MEGA we can implement a useful function that stops the operation of the pump when the well is dry, avoiding the damage of the pump.

6. Document history.

Version	Changes applied	Date	Written	Checked	Approved
1.0.0	First version	04/08/2011	J.M Ibañez	D.Bedford	D.Bedford
1.0.1	Small changes and text modifications	16/08/2011	S.Ureña		
1.0.2	T1 and T2 added in Logic Circuit diagram	29/08/2011	J.M Ibáñez	D.Bedford	D.Bedford
1.0.3	Corrected input connection Figure1 Note about waiting time added PID alarm set to 50%	21/03/2014	JM Ibáñez	J. Català	J. Català