

APPLICATION NOTE	AN-MEGA-0007v105EN
UP/Down with reset function using Customizable Logic of FRENIC MEGA	

Inverter type	FRENIC MEGA
Software version	1000 and later
Required options	Not required
Related documentation	FRENIC MEGA User manual_MEH278a, FRENIC MEGA_Instruction Manual_ INR-SI47-1335-E
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Use	Public, Web
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Version	1.0.5
Languages	English

Introduction.

In FRENIC-MEGA there is no function to reset (set to zero) the speed set point when using UP/DOWN control. This Application Note shows how to reset the speed set point when using UP/DOWN control by using Customizable Logic (function codes UXX) of FRENIC MEGA. This function can be used when the inverter is in STOP mode.

Description.

On one side, in UP/DOWN control when UP or DOWN input functions are active and –at the same time- the speed is changing (during acceleration or deceleration) the inverter takes the actual speed as the speed set point. On the other hand, under UP/DOWN control, the inverter only accepts speed set point changes when RUN signal (Forward or Reverse) is present. From this behaviour, we can expect that if DOWN and RUN Forward input functions are both active and the inverter is in STOP mode then the speed set point becomes zero.

Figure 1 shows the logic circuit diagram of the proposed solution by Customizable Logic. The solution consists in using one digital input (for example X1) for “Speed Reset”; this input is set with NO function (100). As soon as X1 becomes high and the inverter is NOT in RUN2 state (function 1035), DOWN function (18) and RUN Forward command (98) are activated for a short time (pulse time adjusted by Customizable Logic function). As explained before, by activating DOWN and RUN Forward at the same time the speed set point becomes zero because the actual speed is zero (inverter was previously in STOP mode) and therefore resetting the speed set point in UP/DOWN control.

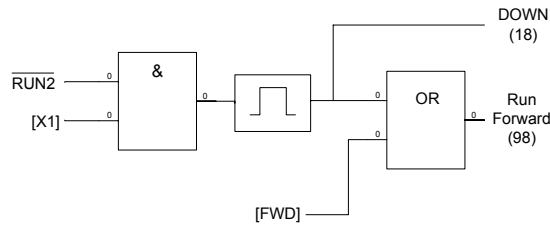


Figure 1. Logic circuit diagram.

Figure 2 shows the input (control) signal connection set up diagram of the proposed solution when the FRENIC MEGA inverter is configured in SOURCE logic.

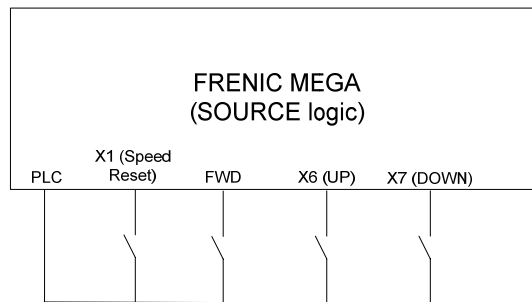


Figure 2. Control signal connection set up diagram (SOURCE logic).

Inverter function set up.

The following table shows the inverter set up from default settings

Function	Value	Description
F01	7	Frequency command 1 by UP/DOWN control
F02	1	Operation command given by FWD or REV
E01	100	No function is assigned to terminal [X1]
E06	17	Terminal [X6] as UP function
E07	18	Terminal [X7] as DOWN function
E98	100	No function is assigned to terminal [FWD]
U00	1	Enable Customizable Logic
U01	2002	Output of step 2 as input 1 signal of step 1
U02	4010	Terminal [FWD] as input 2 signal of step 1
U03	3	OR + General-purpose timer for step 1
U11	1035	Inverse of RUN2 signal as input 1 signal of step 2
U12	4001	Terminal [X1] as input 2 signal of step 2
U13	2	AND + General-purpose timer for step 2
U14	3	Pulse output
U15	0.50 s	Time duration for pulse output

Function	Value	Description
U71	1	Customizable Logic output signal 1 comes from step 1 output
U72	2	Customizable Logic output signal 2 comes from step 2 output
U81	98	Customizable Logic output signal 1 controls the FWD command of the inverter
U82	18	Customizable Logic output signal 2 controls the DOWN command of the inverter

NOTE: When activating X1, the inverter RUN Command will be momentarily activated during 0.5 seconds. Please, take the proper countermeasures against a possible electrical or mechanical accident.

Conclusion.

By using the proposed solution in this document we upgrade the functionality of UP/DOWN control of FRENIC MEGA thanks to the flexibility given by Customizable Logic.

Document history.

Version	Changes applied	Date	Written	Checked	Approved
1.0.0	First version	30/01/2010	D. Bedford		
1.0.1	Some text added	30/04/2010	J. Català		
1.0.2	Some text corrections	04/05/2010	D. Bedford		
1.0.3	NOTE added about safety	05/05/2010	J. Català		
1.0.4	Solution is enhanced. NOTE about safety removed	06/05/2010	D. Bedford		
1.0.5	Inverter function Set up simplified NOTE added about safety	13/05/2010	J. Ibáñez	J. Català	D. Bedford